Si Photonics Technology Platform for High-Speed Optical Interconnect

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Overview

• Luxtera: Introduction

• Silicon Photonics: Introduction

• Silicon Photonics: How it works

• Silicon Photonics: How it Scales to address customer’s needs
Luxtera Company Overview

Luxtera is widely recognized as the industry Leader in Silicon Photonics

- World’s only complete Si Photonics technology platform
- Enables single-chip multiple channel optical transceivers & full SoC integration
- Proven in Volume Production with over 1Mu 10Gb channels
- Sustainable advantages on scalability, density, power, reach, reliability and product cost
Luxtera Market Focus & Products

• Luxtera’s Market Focus:
  Embedded Optics for Data Center, Cloud, Mobile Infrastructure and HPC Equipment
  - High volume embedded optical transceivers for backplanes, networking and high density interconnect

• Luxtera’s Product Portfolio:
  Optoelectronic transceiver chipsets, modules & IP cores for SoC integration
  - Chip-sets: Silicon Photonics Transceiver ICs and companion Light Sources
  - OptoPhy™: Packaged optical transceivers modules
  - Circuit IP for stand alone transceivers and SoC integration
Silicon Photonics: Introduction

Fiber to the Chip
Leverage the vast investments in CMOS technology to achieve low-cost and high-volume capability for photonics:

- Process capability
- High level of integration
- High level of automation

**IC industry methodologies adapted by Luxtera:**

- **Design**
  - Automated Design using standard design tools and qualified Opto-Electronic Design Kit (device libraries, design rules, ...)
  - Extensive design verification prior to tape-out
- **Manufacturing**
  - Emphasis on manufacturability
  - Process monitoring and control
  - Quality & Reliability
Si Photonics – Luxtera: Wafer Processes

**Wafer manufacturing processes:**
- Mature 200 mm process: at Freescale Semiconductor (Austin, TX) 
  Soon available through OpSIS
- Developing 300 mm process at ST Microelectronics (Crolles, France)

**Wafer process allows:**
- Integration of Passive Devices
- Integration of Active devices
- Integration of Photo-detectors
- Integration of Electronics

![Fully Integrated transceiver IC](image)
Silicon Photonics – Luxtera: Design Environment

- Silicon Photonics Design Kit running on Cadence toolset
- Electronic and Photonic Device Library:
  - Parameterized cells
  - Behavioral models built and verified
  - Represent actual process corners
- Automated layout tools
- Design Rule Check (DRC): Process/Device checks + interaction with electronics
- Layout vs Schematic (LVS) Check: E-to-E, E-to-O, and O-to-O connectivity and device extraction
- End-to-end simulation capability
Silicon Photonics: How it works

Fiber to the Chip
Coupling Light In and Out of a Si Photonics Die

Optical I/O through grating couplers:

- Coupling light form light source into die through matched grating coupler
- Coupling TX signals out of die through SMF matched grating coupler
- Coupling RX signals from SMF into die through polarization diversity grating coupler
Wafer-Scale Optical and Electro-Optical Testing

- System based on standard TEL Precio probing system
- Allows 200 mm and 300 mm Silicon Photonics wafer testing
- Wafer-scale testing is key for manufacturing and development
IC Functional Blocks:
- TX: multi-section MZI driven by invertors timed by digital delays, integrated bias control
- RX: Ge WPD with high impedance gain stages
- Programmable pre-emphasis and equalization
- I2C interface for communication and control

4x28 G Transceiver IC Performance:
- Error Free: BER<10^{-15}
- Interoperability with 26-28 G high speed IOs: Altera, Xilinx, Inphi, Gennum (OIF) and others
Reliability of Silicon Devices:
• Inherently reliable (diodes and passives)
• Wear-out conditions are orders of magnitude away from operational conditions

Light Source:
• Proven off-the-shelf InP laser diodes

Reliability Qualifications:
• Silicon Photonics Wafer Process per JEDEC
• Silicon Photonics ICs qualified per JEDEC standard (e.g. HTOL)
• Photonic devices, light source and packaged products per Telcordia GR-468-CORE (with JEDEC sample sizes 😊)
Silicon Photonics: How it scales
SiP is Scalable to Data Rates beyond 56 Gbps NRZ

- **High-Speed Phase Modulator**
  - Intrinsic modulation bandwidth limited by relaxation time ~ 160 GHz
  - Practical limit based on RC time
    - Drive signal rise time 1 ps
    - Rise time optical signal: ~ 5 ps

- **High-Speed Waveguide Photo-Detector**
  - Transit time limited bandwidth
  - Measured electrical (20.log[Iphoto]) bandwidth \( f_0 > 50 \) GHz

- **Electronics**
  - Advanced CMOS nodes will be needed for the electronic circuitry (20 nm)

- **Enables e.g. 64G Fibre Channel**
Si P is Scalable to Long Interconnect Reaches

- 100G needed for spines, not rack top switches
- Reach from rack-top to spine switch is 50-500m
- Overall cost is dominated by cost of optics
- High port density per 1U is desirable
- Customers will deploy the lowest cost solution that meets their requirements

Cost optimized 100-500m solution is critical to success of 100G!

Enabled by Si Photonics single mode infrastructure and light source
Si P is Scalable in Density: PAM-N

- PAM-N under consideration in IEEE standard study groups as low-cost alternative to WDM (LR-4) for 100 GbE
- Si Photonics is ideally suited for PAM-N modulation
- Integrated systems enable performance/power/size optimizations
  - Entire functionality can be integrated into a single transceiver chipset

Example PAM-8 TX-Eye:
- 12 ps Rise/Fall Time
- 8 dB Extinction Ratio
Si P is Scalable in Density: DP-QPSK

- Key blocks can be build from existing device library elements (HSPM, 3 dB splitter, PSGC, PIN PM, Ge WPD, DC)

- Transmitter:
  - IQ Modulator for QPSK
  - PSGC for polarization combiner

- Receiver:
  - PSGC for polarization de-combiner
  - 90 degree hybrids
  - Balanced high-speed receivers with Ge Photo-detectors
Multiple fiber manufacturers explore multicore fibers with excellent results.

Key issue is how to couple light in and out of MCF.

Silicon photonics grating couplers are ideally suited for use with MCF allowing very dense optical interconnect.

MCF in combination with grating couplers allows 100s of optical interfaces on a single die.
Integration of Photonics with Router/Switch

**ROUTER/SWITCH ARCHITECTURES**

- Electronic router
- + Photonic I/O
- + Photonic core

- Electronic switch performance limited by packaging, SerDes, I/O, pins
- Integrated photonic I/O has low power, high bandwidth, long cables
- Integrated core has lower power, area (cost) scale linearly with port count, high bandwidth

OPTICAL INTERCONNECTS FOR HIGH-PERFORMANCE COMPUTING SYSTEMS

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Luxtera’s Photonic Integration Roadmap

CONTEMPORARY:
- MSA compliant Pluggable modules and AOCs: QSFP, CXP,…
- Considerable SI issues (electrical connectors, long traces on host PCBA)

EMERGING:
- Embedded Optical Modules
- Located closer to ASIC to alleviate SI issues (shorter traces)
- Very high reliability required

STRATEGIC DIRECTION:
- Si Photonic Interposer
- SoC Integration
- Smallest form factor
- Lowest system power dissipation
- Very high reliability required
- Use external light source

System Level Power Dissipation per 100 G Port
Summary

- **Silicon Photonics:**
  - Leverages IC design and manufacturing methodologies
  - Is a mature technology in volume production

- **Silicon photonics technology roadmap:**
  - High NRZ data rates w/ long reach: 28 Gbps, 56 Gbps,…
  - Low power: Advanced CMOS Nodes & Integration
  - Higher density: PAM-N, WDM, MCF, DP-QPSK

- **ASIC integration by Silicon Photonic Interposer enables dramatic reduction in system power, size and cost**
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Thank you for your interest.